REMARKS

Claims 1-28 are pending in this application. Claims 1, 9-11, 13-15, 22, 23 and 28 are amended. Claim 8 is canceled. Reconsideration of this application is respectfully requested.

Amendments to the Specification:

Paragraph [0013] has been amended to correct a clerical error and to correct "senor" to read as "sensor."

Claim Amendments

Claim 1 has been amended to incorporate the features recited in original Claim 8 (now canceled). Also, Claim 1 has been amended to recite that an inverter is coupled to an output terminal of the sensor; that the device is coupled to the voltage divider "in series" and that the high state voltage is applied to the inverter. Support for the amendments can be found at, for example, Paragraphs [0012]-[0015] and FIG. 2.

Claim 9 has been amended to depend from Claim 1 and to better recite that "an output" of the inverter is coupled to an ESD protection. Support for the amendments can be found at, for example, Paragraph [0019] and FIG. 3.

Claim 13 has been amended to recite that the MOS transistor is configured to discharge an ESD pulse and that the sensor applies the high state voltage to an input terminal of the inverter. Support for the amendments can be found at, for example, Paragraphs [0020], [0024]-[0027] and FIG. 3.

Claim 23 has been amended to recite that the MOS transistor is configured to discharge the ESD pulse. Support for the amendment can be found at, for example, Paragraphs [0024]-[0027] and FIG. 3.

Claims 10, 11, 14, 15, 22 and 28 have been amended for consistency with the amendments of Claims 9, 13 and 28.

No new matter is added.

Rejection under 35 U.S.C. §112, second paragraph

The Action rejects Claim 1 under 35 U.S.C. §112, second paragraph for being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention because the phrase "voltage divider" is indefinite. Applicants respectfully disagree.

As know in the art, a voltage divider is used to create a voltage (e.g., an output voltage) which is proportional to another voltage (e.g., an input voltage). As described in the specification, the voltage divider can be a series of diodes, a resistor, transistors or any other equivalent circuit. The Examiner questions how a series a diodes can form a voltage divider. As one of ordinary skill in the art will recognize, a diode has a voltage drop across its terminals when conducting. Therefore, when conducting, the diodes can be viewed as a resistive element. The same holds true for a series of diodes. Therefore, it is submitted that the claims particularly point out and distinctively claim the invented subject matter. Withdrawal of the §112, second paragraph rejection is respectfully requested.

Claims Rejections under 35 U.S.C. §102(b)

Dungan et al.

The Action rejects Claims 1-10 and 13-21 under 35 U.S.C. §102(b) for being anticipated by U.S. Patent No. 5,311,391 to Dungan et al. ("Dungan").

Claim 1 has been amended to recite that that the device is coupled to the voltage divider "in series" and that the high state voltage is applied to the inverter. Applicants submit that Claim 1 is not anticipated by Dungan as described below.

Dungan discloses an ESD protection circuit. In this Action, the Examiner refers to series diodes 51a-51e as the voltage divider of Claim 1 and diode 51f as the device recited in Claim 1. As shown in Dungan's FIG. 2, the voltage of output node 53 is applied to **gate 55 of trigger FET 57.** Nothing in Dungan's description or drawings shows that the voltage of output node 53 is applied to an inverter.

During an ESD event, Dungan applies a high voltage to gate 55 of trigger FET 57 to turn on trigger FET 57 so that **the voltage on inverter node 61 is pulled down** until shunt FET 47 turns on. (Col. 4, Lines 40-55). Accordingly, without applying the high voltage on output node 53 to gate 55 of trigger FET 57, the ESD current cannot be shunted from bus 17 through shunt FET 47 to ground plane 41. Therefore, Applicants submit that Dungan fails to teach or suggest applying a high state voltage to the inverter. Therefore, Claim 1 is not anticipated by Dungan.

Claims 2-7, 9 and 10 depend from Claim 1 and are, therefore, also not anticipated by Dungan.

Clam 13 has been amended to recite that the sensor applies the high state voltage to the input terminal of the inverter. For reasons analogous to the arguments set forth above in connection with Claim 1, Dungan fails to disclose or suggest this claimed feature. Applicants submit that Claim 13, therefore, is not anticipated by Dungan.

Claims 14-21 depend from Claim 13 and are also not anticipated by Dungan via virtue of their dependency.

Yu

The Action also rejects Claims 1, 8-10 and 13, 14, 23-28 under 35 U.S.C. §102(b) for being anticipated by U.S. Patent No. 6,014,298 to Yu ("Yu").

Claim 1 has been amended to recite that the device adapted to maintain the high state voltage at the output of the sensor is coupled to the voltage divider in series. Applicants submit that Yu fails to show the claimed feature.

In rejecting Claim 1, the Action refers to the combination of resistor R2 and capacitor C2 of FIG. 4 of Yu as the voltage divider, and inverter 30 as the "device coupled to the voltage divider." Inverter 30 is coupled to the node **between** resistor R2 and capacitor C2. Clearly, resistor R2 and capacitor C2 are **not** coupled to inverter 30 **in series.**

When an ESD event occurs, Yu seeks to apply a voltage to the gate of NMOS transistor M2 so as to turn on NMOS transistor M2, as shown in FIG. 4. (Col. 4, Line 65 – Col. 5, Line 7).

Two diode inverters 30 and 32 shown in FIG. 4 are coupled in series between the gate of NMOS transistor M2 and the node between resistor R2 and capacitor C2 such that **the same voltage state on the node between resistor R2 and capacitor C2 can be applied to the gate of NMOS transistor M2**. The circuit would not operate in this manner if resistor R2 and capacitor C2 were coupled in series with inverter 30. Therefore, it is submitted that Claim 1 is not anticipated by Yu.

Claims 9 and 10 depend from Claim 1 and are, therefore, also not anticipated by Yu.

Claim 13 has been amended to recite that the MOS transistor is configured to discharge an ESD pulse. Applicants submit that Yu fails to teach or suggest this claimed feature.

Yu uses delay circuit 282 (i.e., resistor R2, capacitor C2 and inverters 30, 32 (FIG. 4)) to turn on/off switch 281 (i.e., NMOS transistor M2) in order to control the voltage applied to internal circuitry 22. (FIG. 2, Col. 3, Lines 6-16 and Col. 3, Lines 50-64). When an ESD event occurs, NMOS transistor M2 is turned off to **block** the ESD pulse from being applied to **internal circuitry 22**. In the absence of an ESD pulse, NMOS transistor M2 is turned on such that a normal operating voltage can be applied to internal circuitry 22. (Id.) Clearly, NMOS transistor M2 is **NOT** configured to discharge an ESD pulse. Accordingly, Yu fails to teach or suggest that the MOS transistor is configured to discharge an ESD pulse as claimed in Claim 13. Applicants submit that Claim 13 is not anticipated by Yu and is, therefore, allowable for at least the reasons set forth above.

Claim 14 depends from Claim 13 and is also allowable.

Claim 23 has been amended to recite that the MOS transistor is configured to discharge an ESD pulse. For reasons analogous to those set forth above in connection with Claim 13, it is submitted that Claim 23 is not anticipated by and is allowable over Yu.

Claims 24-28 depend from Claim 23 and are, therefore, also not anticipated by Yu.

From the foregoing, Claims 1-7, 9, 10, 13-21 and 23-28 are not anticipated by the art of record and are, therefore, allowable for at least the reasons set forth above. Reconsideration and withdrawal of the 102(b) rejections are respectfully requested.

Claims Rejections under 35 U.S.C. §103(a)

The Action also rejects Claims 11, 12 and 22 as being obvious from Yu in view of U.S. Patent No. 6,775,112 to Smith et al. ("Smith").

Claims 11, 12 and 22 depend from Claims 1 and 13. For at least the reasons set forth above, it is submitted that these claims are allowable.

In accordance with the foregoing arguments and amendments, reconsideration and withdrawal of the rejections of Claims 1-7 and 9-28 are respectfully requested.

Conclusion

Applicants submit that this application is in condition for allowance. Early notification to that effect is respectfully requested.

The Commissioner for Patents is hereby authorized to charge any additional fees or credit any excess payment that may be associated with this communication to deposit account **04-1679.**

Respectfully submitted,

Dated: 12-15-2006

Joseph A. Powers, Reg. No.: 47,006
Attorney For Applicants

DUANE MORRIS LLP
30 South 17th Street
Philadelphia, Pennsylvania 19103-4196
(215) 979-1842 (Telephone)
(215) 979-1020 (Fax)